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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,474	12/12/2003	Kit Fai Chan	M4065.0741/P741	8825

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EXAMINER	
BARTON, JONATHAN A	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,474	CHAN ET AL.	
	Examiner	Art Unit	
	Jonathan Barton	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-11 and 13-25* is/are rejected.

7)☒ Claim(s) *2-5, 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 7 and 11 are objected to because of the following informalities:

a. In claim 7 "said four transistor" should read "said fourth transistor".

b. In claims 11 and 22 the semicolons at the end of the claims need to be periods.

c. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. Claim 19 recites the limitation "second bias current *source*" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 6-10, 16, and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Evans et al. (US 6,442,054).

d. As for claims 1, 10 and 21 Evans et al. disclose

i. a matchline (Col. 1 Lines 35-37);

ii. a plurality of content addressable memory cells, coupled to said matchline (Col. 1 Lines 60-65);

iii. a first current source, coupled to the matchline (Col. 1 Lines 35-37); and

iv. a second current source, coupled to the matchline (Col. 1 Lines 49-53);

v. wherein said first current source is biased to supply a first current to the matchline and to the second current source, and said second current source is biased to supply a second current, said first current being greater than said second current (Col. 3 Lines 34-44).

e. As for claims 6 and 16 Evans et al. disclose

vi. a first transistor, coupled to a power source (Col. 3 Lines 17-20);

vii. a second transistor, coupled to said first transistor and to the matchline (Col. 3 Lines 17-20);

viii. wherein said second transistor has a gate terminal coupled to a bias circuit (Col. 3 Lines 21-24).

f. As for claim 7 Evans et al. disclose

ix. a third transistor, coupled to the power source (Col. 3 Lines 19-20);

x. a fourth transistor, coupled to said third transistor, and coupled to the gate of said second transistor (Col. 3 Lines 19-24); and

xi. a first bias current source coupled said fourth transistor and to ground; wherein said gate of said four transistor is also coupled to a

source/drain terminal of said fourth transistor which is coupled to a terminal of said first bias current source (Col. 3 Lines 21-24).

g. As for claims 8 and 18 Evans et al. disclose

xii. said second current source comprises: a first transistor, coupled to the matchline (Col. 3 Lines 17-20);

xiii. a second transistor, coupled to said first transistor and to ground; wherein said first transistor has a gate terminal coupled to a bias circuit (Col. 3 Lines 17-20).

h. As for claims 9 and 19 Evans et al. disclose

xiv. a second bias current source coupled to a power source (Col. 3 Lines 21-24);

xv. a third transistor coupled to said second bias current source and coupled to the gate of said first transistor (Col. 3 Lines 19-20); and

xvi. a fourth transistor, coupled to said third transistor and to ground (Col. 3 Lines 19-24).

i. As for claim 20 Evans et al. disclose

xvii. a plurality of network interface devices, each of said network interface devices coupled to said processor, wherein said system routes network traffic between the plurality of network interface devices (Col. 4 Lines 39-49).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11, 13-15, 17 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans et al. (US 6,442,054) in view of Kurihara et al. (US 6,381,163).

j. As for claim 11 Evans et al disclose:

xviii. a first current mirror, coupled to said first current source (Col. 2 Lines 11-16);

xix. a second current mirror, coupled to said second current source (Col. 3 Line 65 – Col. 4 Line 6);

k. Evans et al fail to disclose the following limitation, which is taught by Kurihara et al:

xx. a current measurement circuit, coupled to said first current mirror and said second current mirror (Col. 2 Line 63 – Col. 3 Line 2).

xxi. It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the current measurement circuit taught by Kurihara et al. with the content addressable memory disclosed by Evans et al. because both systems are content addressable memories and Kurihara's current measurement circuit is disclosed as being common practice within the art, which makes it an obvious choice for use.

l. As for claim 13 Kurihara et al. teach

xxii. said current measurement circuit outputs a voltage reflecting a magnitude of a sense current flowing from said first current source (Col. 2 Lines 60-63). See paragraph xxi above for combinational motivation logic.

m. As for claim 14 Kurihara et al. teach

xxiii. said measurement circuit comprises a first inverter, coupled to said first current mirror and said second current mirror (Col. 6 Lines 13-16). See paragraph xxi above for combinational motivation logic.

n. As for claim 15 Kurihara et al. teach

xxiv. said measurement circuit further comprises: a second inverter, coupled in series with said first inverter (Col. 6 Lines 13-16). See paragraph xxi above for combinational motivation logic.

o. As for claim 17 Evans et al. disclose

xxv. a third transistor, coupled to the power source (Col. 3 Lines 19-20);

xxvi. a fourth transistor, coupled to said third transistor and coupled to the gate of said second transistor (Col. 3 Lines 19-24); and

xxvii. a first bias current source coupled said fourth transistor and to ground (Col. 3 Lines 21-24).

p. As for claim 22 Kurihara et al. teach

xxviii. measuring said first current to determine a state of a plurality of CAM cells coupled to said matchline (Col. 6 Lines 21-27). See paragraph xxi above for combinational motivation logic.

q. As for claim 23 Kurihara et al. teach

xxix. said measuring step comprises: measuring a third current flowing between a first current mirror and a measurement circuit (Col. 2 Line 56 – Col. 3 Line 2);

r. while Evans et al. disclose

xxx. wherein a first current mirror is coupled to said first current source and configured to produce the third current, said third current having the same magnitude as said first current (Col. 2 Lines 11-16). See paragraph xxi above for combinational motivation logic.

s. As for claim 24 Kurihara et al. teach

xxxi. said measuring step indicates that the matchline is in a first logical state when said third current is equal to said first bias current (Col. 6 Lines 21-22). See paragraph xxi above for combinational motivation logic.

t. As for claim 25 Kurihara et al. teach

xxxii. measuring step indicates that the matchline is in a second logical state when said third current is equal to said second bias current (Col. 6 Lines 26-27). See paragraph xxi above for combinational motivation logic.

Allowable Subject Matter

7. Claims 2-5 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

u. Claims 2 and 12 contain at least the following allowable subject matter:

xxxiii. wherein said first current mirror is coupled to said first current source and configured to supply a third current mirroring said first current to said measurement circuit and said second current mirror, and

xxxiv. said second current mirror is coupled to said second current source and configured to supply a fourth current mirroring said second current.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan Barton whose telephone number is 571-272-8157. The examiner can normally be reached on Monday - Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jonathan Barton
Examiner
Art Unit 2186

JB

JB

PRIMARY ~~EXAMINER~~
GROUP 2100